Nuclei RISC-V Processor

NA900 Product Brief

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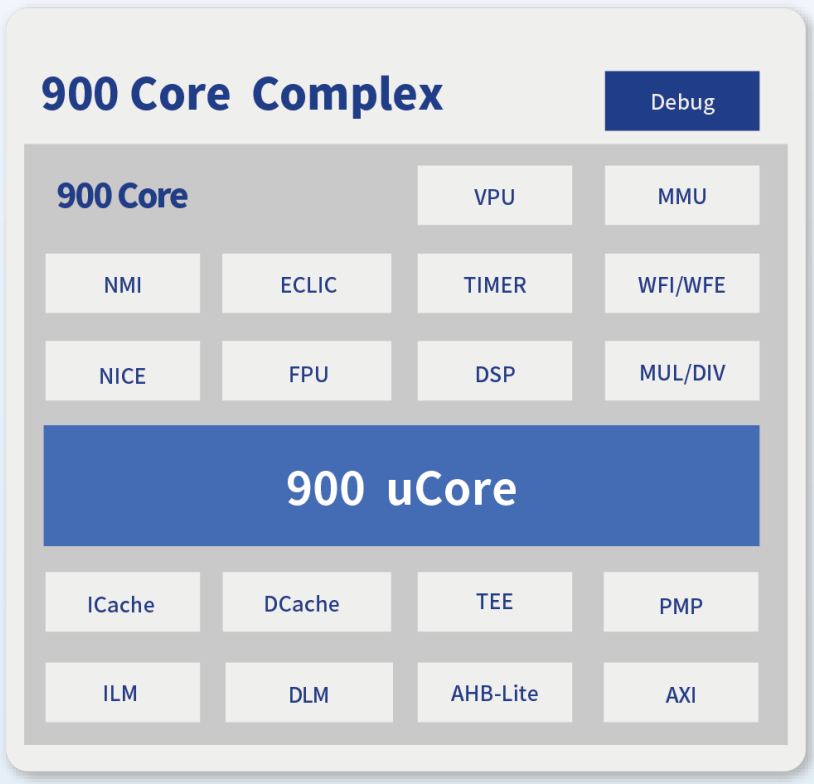
Overall Introduction

Nuclei NA900 is a high-performance processor based on RISC-V architecture. NA900 features a **dual-issue 9-stage in-order execution pipeline.** NA900 is the 1st RISC-V CPU IP that achieves ISO 26262 ASIL-D product certificate. The certificate is accomplished together with Exida.

As a high-performance, **NA900** gives 2.78/5.99(legal/best) Dhrystone/MHz, 5.23 Coremark/MHz.



NA900 supports both instruction and data local memory **(ILM/DLM)** gives better real time processing capability. User can also configure instruction and data cache **(I-Cache/D-Cache)** to improve the performance of the overall subsystem.

NA900 supports **Dual-Core Lockstep Mode** for ASIL-D functional safety requirement with 99% single point coverage. Meanwhile, NA900 can be configured as **Dual-Core Split Mode**, with each core working separately on ASIL-B level, delivering higher performance. Split Mode **can be configured through software**, giving customer huge flexibility during system level design.

NA900 aims for automotive application and is already deployed in **Engine ECU, ADAS, Gateway and Lidar.** NA900 is comparable to ARM Cortex-R52.

High Performance
Real-time Capability

RV32/64IMACFDP
VBZfh

9-stage Pipeline

Support
I/DCache

Machine Mode
User Mode
Supervisor Mode

Dual Core Lock Step
Dual Core Split

ASIL-D

AXI
System Bus

RISC-V
Standard Debug

4-Wire JTAG
2-Wire cJTAG

Low Latency
Interrupt

Full Dev Kit & SDK

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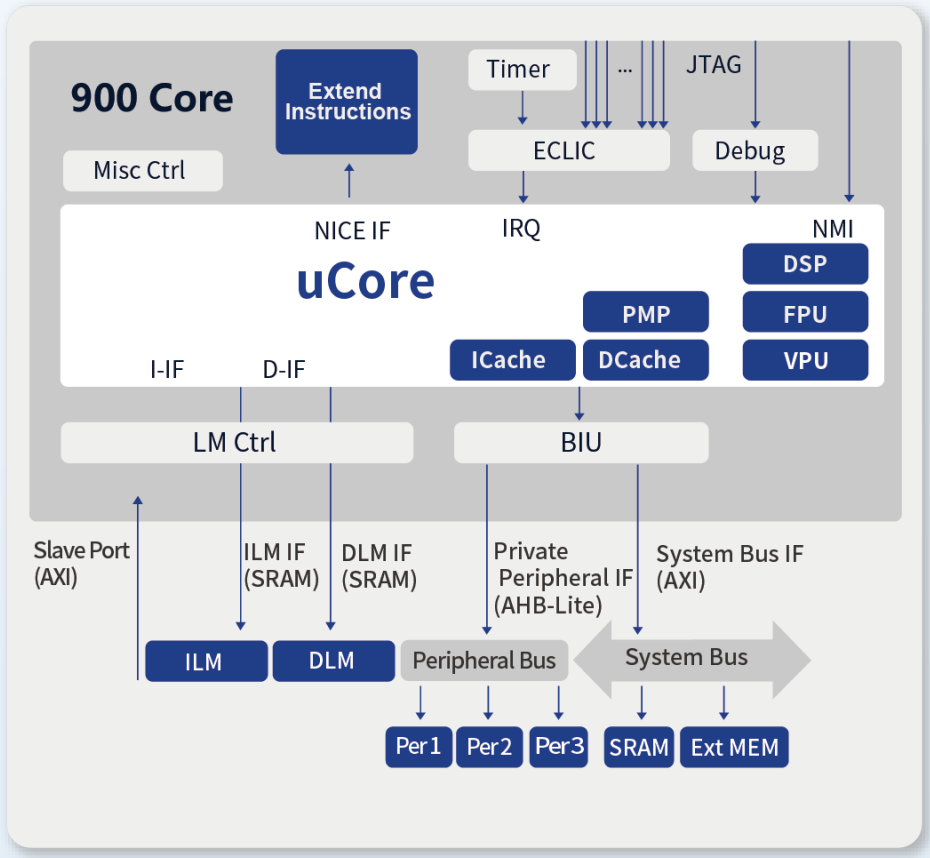
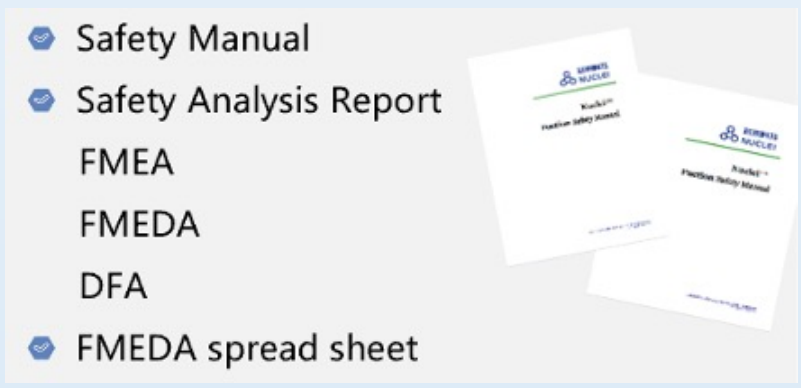
NA900 Feature

- ISO26262 ASIL-D product certified, excellent for Automotive and Functional Safety application;
- **RV32IMACFDPB** compatible, 9-stage in order **dual-issue** pipeline;
- Support **64b** AXI system interface， 32b AHB-Lite private peripheral interface and ILM/DLM interface;
- **Double/Single Precision** floating point and **DSP** Extension;
- Configurable ILM **(Instruction Local Memory)** & DLM**(Data Local Memory)** with **ECC**;
- Configurable **I-Cache** with Scratchpad mode & **D-Cache** with **ECC**;
- Configurable **PMP** and **TEE (Trust Execution Environment)** for **system security**;
- Support standard **JTAG & cJTAG** interface and Linux/Windows debug tools;
- Support standard RISC-V GNU toolchain and Linux/Windows dev environment (**IDE**)





NA900D Serires

Systematic Capability:ASIL D
Hardware Safety Integrity: ASIL D in DCLS mode

- **World First ISO 26262 ASIL-D certified RISC-V CPU IP**

exida

Certificate / Certificat
Zertifikat / 合格証

Nuclei 21/06-003 C001

exida hereby confirms that the:

NA900 Processor

Nuclei System Technology Co., Ltd.
Shanghai, P.R. China

The manufacturer may use the mark:

Has been assessed per the relevant requirements of:

ISO 26262:2018 Parts 2, 4, 5, 7, 8 and 9

and meets the requirements providing a level of integrity to:

ASIL D

Safety related function:
The NA900 Processor was developed as a HW Safety Element out of Context (SEooC), with the following assumed top-level safety requirements for a safety related application context:

- Safe computation (including execution of the defined ISA, handling of interrupts and external events, privilege mode access protection, memory access protection and low power mode management, etc.)
- Protect the data integrity of all safety related SRAM storage and transfer between core and SRAM
- Provide safe communication through the bus interfaces
- Correctly indicate the processor status through external miscellaneous output signals

Application restrictions:
The NA900 processor shall be used according to the requirements described in the Nuclei NA900 Processor Safety Manual.

Revision 1.0 Jul 17, 2023
Surveillance Audit Due Aug 1, 2026

Evaluating Assessor

Certifying Assessor

Page 1 of 2

NA900B Series

Systematic Capability:ASIL D
Hardware Safety Integrity: ASIL B

- **Nuclei self developed Softwate Test Library for ASIL B application**
- **Fault Injection simulation FMEDA report for configurable design**
- **ASIL B support fot both split mode and single-core mode**
- **Safety enhanced hardware for trade-off between diagnostic coverage and hardware cost**

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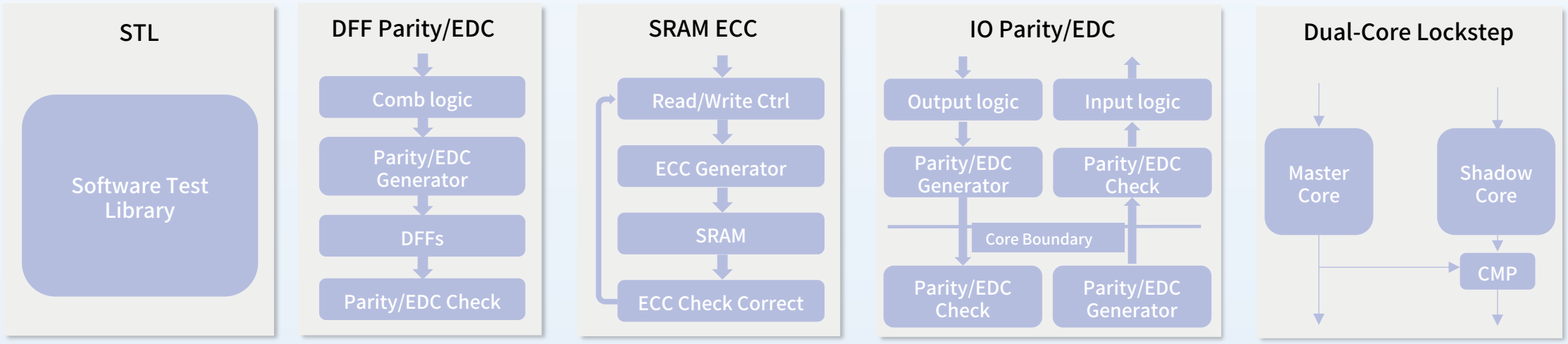
Functional Safety (ASIL-B & ASIL-D)



Providing STL(software test library)

Implementing error detection code (EDC) on core DFF. Selective coverage of architectural, pipeline or all DFF.

Implementing error correction code (ECC) on ILM, DLM, I/D-Cache with enhanced address and multi-bit error coverage

Implementing error detection code (EDC) on core boundary IO

The Dual-core lockstep cores executing the same code, then their outputs and key internal states are compared every cycle; Any mismatch will generate a fault by the comparison unit

Automotive Safety Integrity Levels

QM A B C D

Safety Package

FMEDA

o	Block / Subblock [Drop-down]:	Block / Component	Block / Component Group	High Level Block / Component Group	$\lambda_{permanent}$ [FIT]	Failure Mode (FM) for the block	FM distribution permanent	FM distribution transient
1	Master core	master core	-	-	4.7720	All applicable failure mode of computation or communication execution caused by faults in the master core (100) logic	97.0%	99.0%
1	Master core	master core	-	-	4.7720	Unexpected ECC error detection:1. Detect error when not expected (false alarm).2. Not detect a true ECC error.	1.0%	0.5%
1	Master core	master core	-	-	4.7720	Generate wrong ECC code to the SRAM write data bus	1.1%	1.1%
1	Master core	master core	-	-	4.7720	Unexpected SBE correction: 1. Do correction on correct data and result in data error. 2. missing a true SBE correction	1.0%	1.0%

	Top level safety requirements (TLSRs) on IP / IC Level	*TLSR short*	SPFM	LFM
1	NA900 shall provide the required safe computation	TLSR 01	99.996%	99.784%
2	NA900 shall protect the data integrity of all safety related SRAM Storage and transfer between core and SRAM.	TLSR 02	99.268%	98.885%
3	NA900 shall provide safe communication through the bus interfaces	TLSR 03	99.996%	99.784%
4	NA900 shall be configured through external miscellaneous input signals, and correctly indicate the processor status through external miscellaneous output signals.	TLSR 04	99.996%	99.784%

Safety Manual

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NA900 Memory Subsystem

900 Series supports local instruction and data memory: **ILM (Instruction Local Memory) 和DLM (Data Local Memory)**, providing real-time processing capability:

- ILM and DLM can be configured from **128B-2GB**, allowing excellent flexibility;
- **AHB-Lite interface and SRAM interface** with customized **address space.**

900 Series supports Instruction Cache

- **2-way, 64B cache line** structure
- Cache size from **8KB-64KB**
- Support cache line **LOCK and INVAL** operation

900 Series supports Data Cache

- **2-way, 64B cache line** structure
- Cache size from **8KB-64KB**
- Support cache line **LOCK and INVAL** operation

900 Series System Interface Introduction

Bus Interface	Description	Atomic Support	Burst Support	Cacheablility	Protocols	Bus Width
System Bus	System Instruction and Data	Yes	Yes	Configurable	AXI4	64 bit
ILM Interface	Local Instruction	No	No	No	SRAM	64 bit
DLM Interface	Local Data	No	No	No	SRAM	2*32 bit
PPI Interface	Private Peripherals	No	No	No	AHB-Lite	32 bit
Slave Interface	External Master Read	No	Yes	No	AXI4	64 bit

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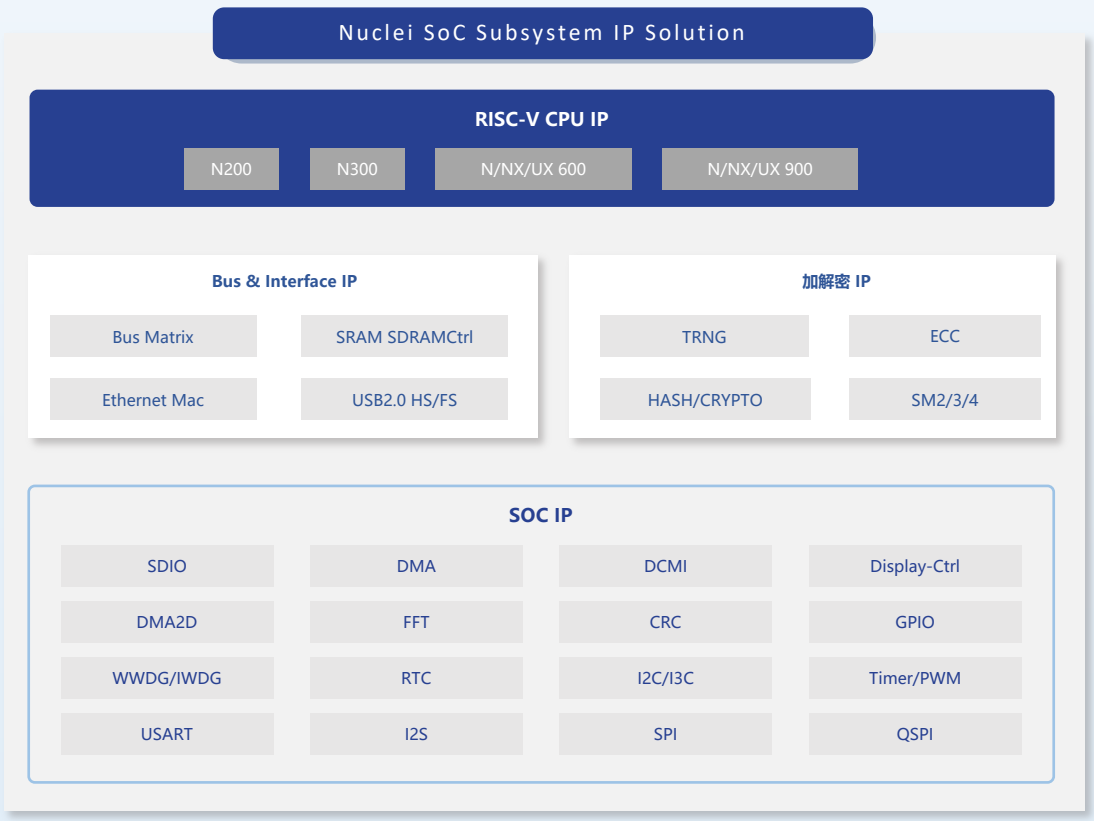
Nuclei CPU Subsystem

Using internal tools from Nuclei to integrate CPU IPs with other peripheral IPs , verify and deliver **a full subsystem solution** to customer.

- Save money：Full subsystem IP **reduces customer’ s cost**;
- Save time：Pre-integrated SoC subsystem **saves customer’ s development cycle**;
- Save effort：Related SoC driver and SDK help **fast prototype bring up**.

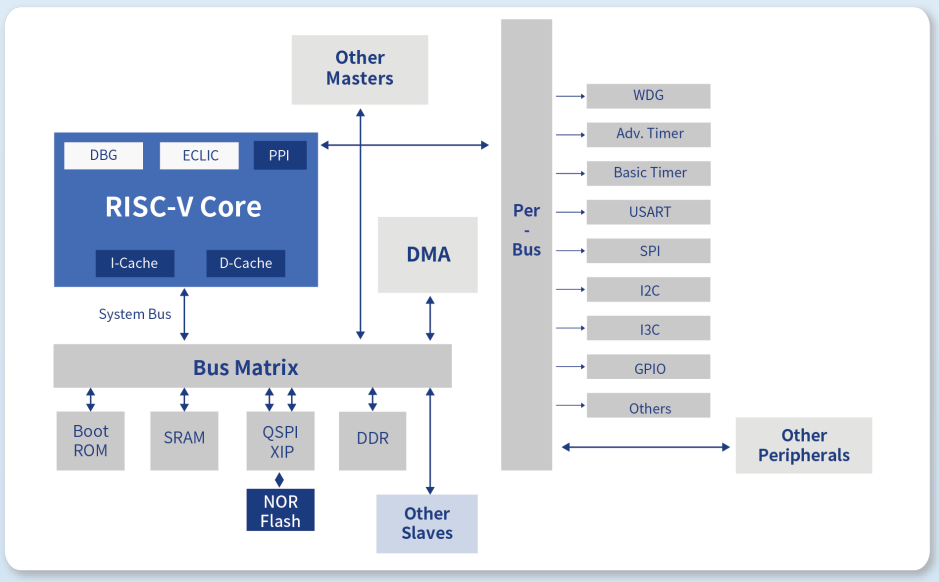


Innovative Subsystem IP Use Case

Use Case #1

Single-core：

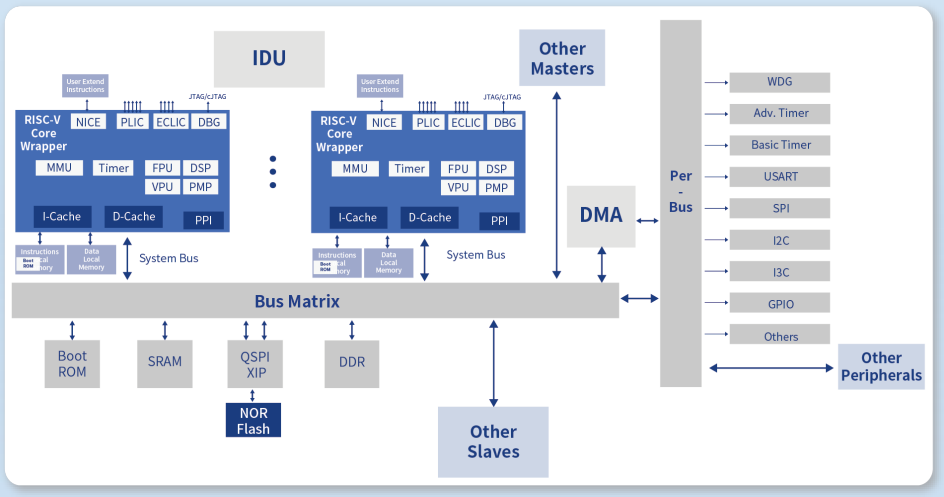
Customer succeeded to **bring up in 2 weeks** based on delivered IP package & SDK



Use Case #2

Multi-core：

Supported two modes **(real-time & application),** including IDU, bus matrix, etc.



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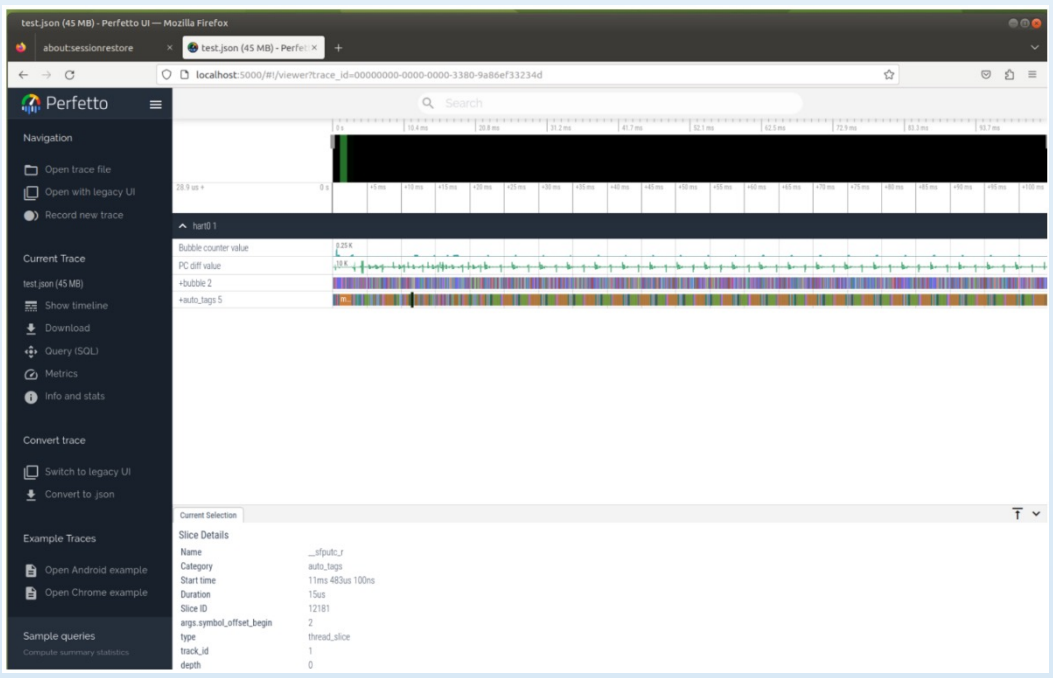
Nuclei IDE

Eclipse CDT Based development environment, easy hands on with manual.

- Nuclei RISC-V GCC, OpenOCD and QEMU integrated
- Nuclei Package(NPK) software solution
- Support SoC Subsystem SDK one-click import
- Portable executables, without installation
- One-click project template
- One-click project configuration
- In system debugging and programming
- Integrated serial port tool
- Real time register display
- Support Linux and Windows
- Deeply integrated with RV Prof – professional **performance profiling and optimizing tool**, instruction and cycle level accurate
- Embedded with **RISC-V e-trace**，debug and analyze performance with ATB2AXI module and trace decoder



NA900 Series Has Been Deployed to Automotive Applications

ADAS　Lidar　Engine ECU

MCU　Gateway　Computing