Nuclei RISC-V Processor

# NA300 Product Brief

# Nuclei NA300 Product Brief

芯来科技 NUCLEI

## Overall Introduction

Nuclei NA300 is a processor based on RISC-V architecture, which achieves ISO 26262 ASIL-D Product Certificate. The certificate is accomplished together with German exida.

Nuclei NA300 features a 3-stage, dual issue in order pipeline that is compatible with RV32IMACFDBPC/Zcxlcz. NA300 delivers 1.5 Dhrystone/MHz, 3.4 Coremark/MHz.


NA300 supports both instruction and data local memory (ILM/DLM) gives better real time processing capability. User can also configure instruction and data cache (I-Cache/D-Cache) to improve the performance of the overall subsystem.

NA300 aims for automotive application and is already deployed in Engine ECU. NA300 is comparable to ARM Cortex-M33.

- Extreme Cost Effective
- RV32 IMACFDPB
- 3-stage Pipeline Single/Dual Issue Configurable
- Support I/D-Cache
- PMP and TEE Security Features
- Single/Double Precision FP and SIMD DSP Unit
- ASIL-D Ready
- AHB-Lite System Bus
- RISC-V Standard Debug
- 4-Wire JTAG 2-Wire cJTAG
- Low Latency Interrupt
- Full Dev Kit & SDK

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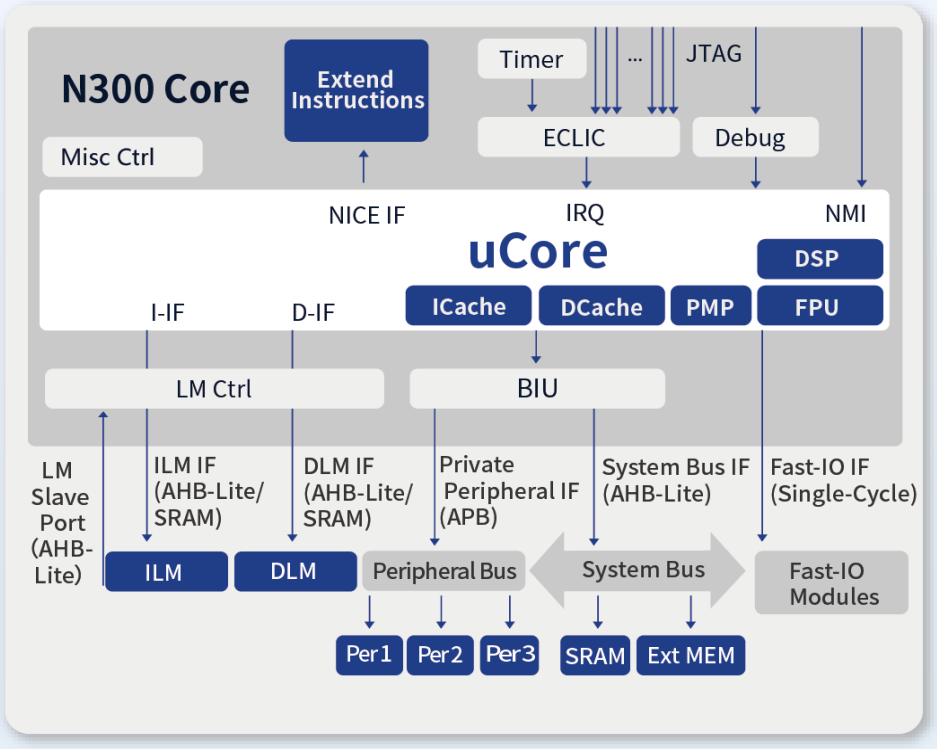
## NA300 Feature

- ISO26262 ASIL-D systmatic capability, excellent for Automotive and Functional Safety application;
- RV32IMACFDBPC/Zcxlcz compatible，3-stage, dual issue in order pipeline;
- Support 32b AHB bus interface，32b AXI Slave Port and ILM/DLM interface;
- Double/Single Precision floating point and DSP Extension;
- Configurable ILM (Instruction Local Memory) & DLM(Data Local Memory) with ECC;
- Configurable I-Cache & D-Cache with ECC;
- PMP and TEE (Trust Execution Environment) configurable;
- Support standard JTAG & cJTAG interface and Linux/Windows debug tools;
- Support standard RISC-V GNU toolchain and Linux/Windows dev environment (IDE)




- Safety Manual
- Safety Analysis Report
  - FMEA
  - FMEDA
  - DFA
- FMEDA spread sheet

## NA300D Serires

***Systematic Capability:ASIL D***
***Hardware Safety Integrity: ASIL D in DCLS mode***

exida

Certificate / Certificat
Zertifikat / 合格証

Nuclei 23/09-103 C001

*exida* hereby confirms that the:

**NA300 Processor**

**Nuclei System Technology Co., Ltd.**
**Shanghai, P.R. China**

Has been assessed per the relevant requirements of:

**ISO 26262:2018 Parts 2, 4, 5, 7, 8 and 9**

and meets the requirements providing a level of integrity to:

**ASIL D**

**Safety related function:**
The NA300 Processor was developed as a HW Safety Element out of Context (SEooC), with the following assumed top-level safety requirements for a safety related application context:

- Safe computation
- Safe data storage and transfer
- Safe communication
- Correctly indicate the processor status

**Application restrictions:**
The NA300 processor shall be used according to the requirements described in the Nuclei NA300 Processor Safety Manual.

The manufacturer may use the mark:

CERTIFIED exida ISO 26262 ASIL D

Revision 1.0 Jun 24, 2024
Surveillance Audit Due Jul 1, 2027

ANAB ANSI National Accreditation Board ACCREDITED ISO/IEC 17065 PRODUCT CERTIFICATION BODY #1004

exida Certification

Evaluating Assessor

Certifying Assessor

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## NA300B Series

***Systematic Capability:ASIL D***
***Hardware Safety Integrity: ASIL B***

- Nuclei self developed Softwate Test Library for ASIL B application
- Fault Injection simulation FMEDA report for configurable design
- ASIL B support fot both split mode and single-core mode
- Safety enhanced hardware for trade-off between diagnostic coverage and hardware cost

## NA300 Memory Subsystem

N300 Series supports local instruction and data memory: ILM (Instruction Local Memory) 和DLM (Data Local Memory), providing real-time processing capability:

- ILM and DLM can be configured from 128B-2GB, allowing excellent flexibility;
- AHB-Lite interface and SRAM interface with customized address space.

N300 Series supports Instruction Cache

- 2-way, 32B cache line structure
- Cache size from 1KB-64KB
- If ILM is not configured, I-Cache can be configured to Scratchpad Mode through CSR
- Support cache line LOCK and INVAL operation

N300 Series supports Data Cache

- 2-way, 32B cache line structure
- Cache size from 1KB-64KB
- Support cache line LOCK and INVAL operation

## NA300 System Interface Introduction

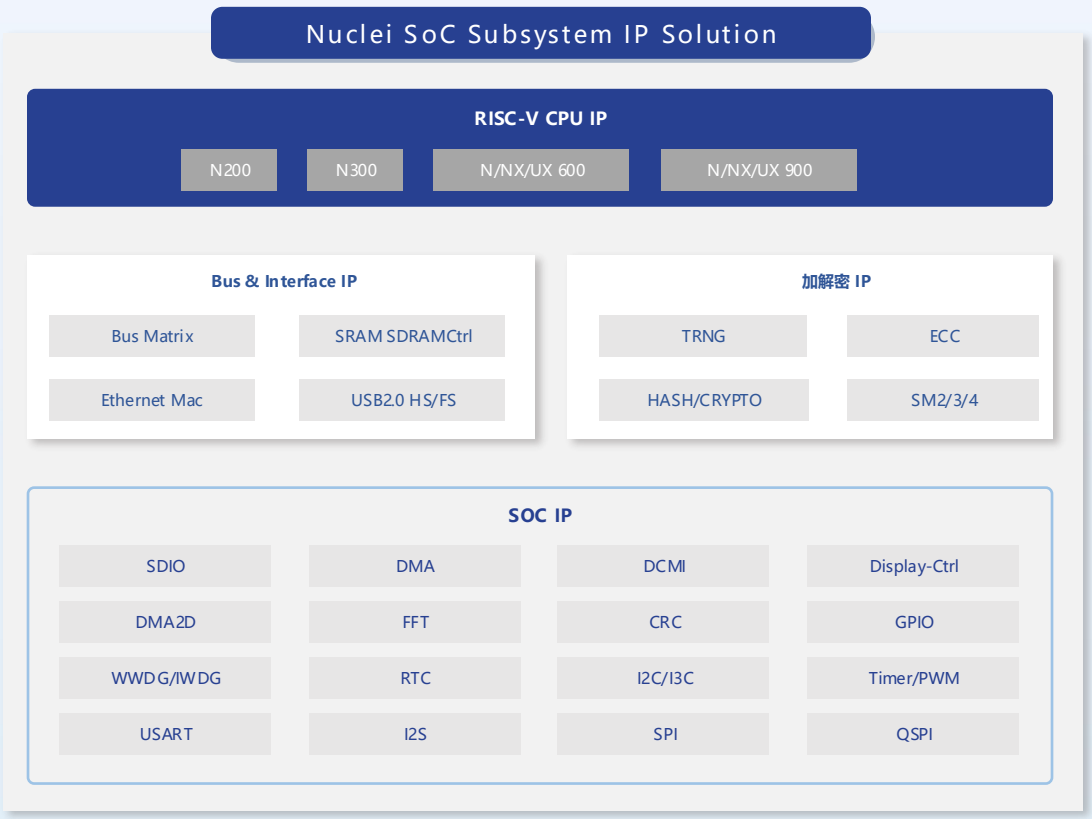
| Bus Interface | Description | Atomic Support | Burst Support | Cacheablility | Protocols | Bus Width |
|---|---|---|---|---|---|---|
| System Bus | System Instruction and Data | Yes | Yes | Configurable | AHB-Lite | 32 bit |
| I-Cache Bus | Used for I-Cache miss | No | Yes | Configurable | AHB-Lite | 32 bit |
| ILM Interface | Local Instruction | No | No | No | SRAM/ AHB-Lite | 32 bit |
| DLM Interface | Local Data | No | No | No | SRAM/ AHB-Lite | 32 bit |
| PPI Interface | Private Peripherals | No | No | No | AHB-Lite | 32 bit |
| Slave Interface | External Master Read | No | No | No | AHB-Lite | 32 bit |

# Nuclei NA300 Product Brief

## Nuclei CPU Subsystem

Using internal tools from Nuclei to integrate CPU IPs with other peripheral IPs , verify and deliver a full subsystem solution to customer.

- Save money：Full subsystem IP reduces customer’s cost;
- Save time：Pre-integrated SoC subsystem saves customer’s development cycle;
- Save effort：Related SoC driver and SDK help fast prototype bring up.

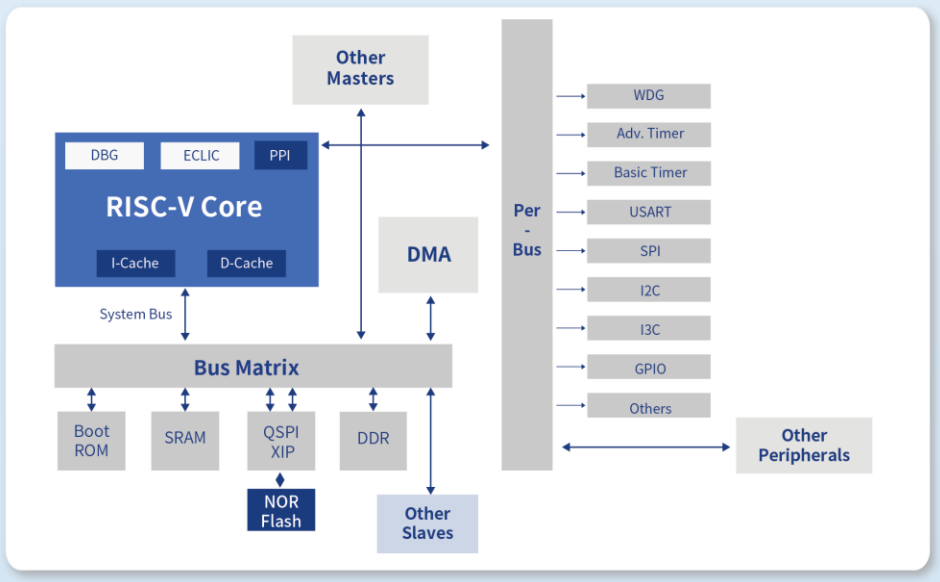



## Innovative Subsystem IP Use Case

### Use Case #1

Single-core：

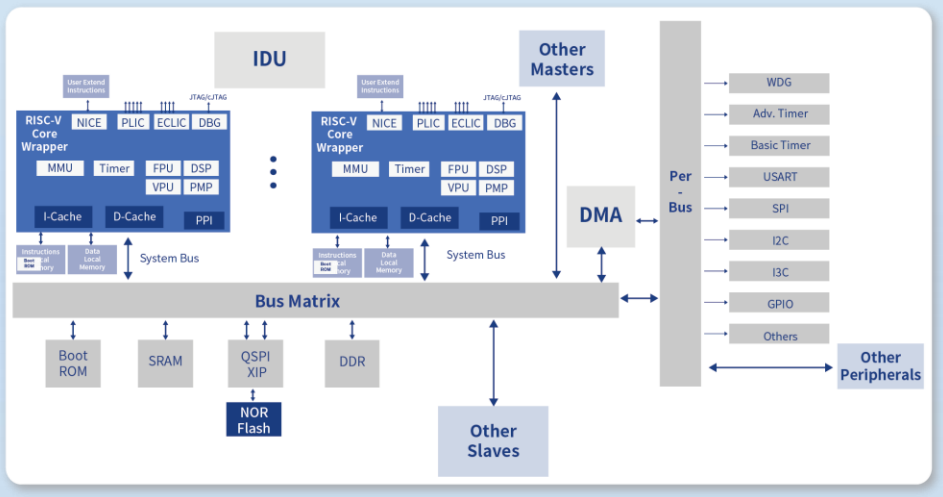
Customer succeeded to bring up in 2 weeks based on delivered IP package & SDK




### Use Case #2

Multi-core：

Supported two modes (real-time & application), including IDU, bus matrix, etc.



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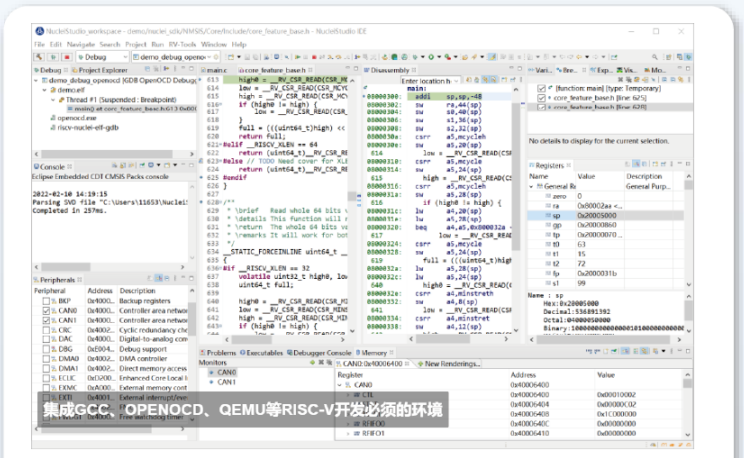
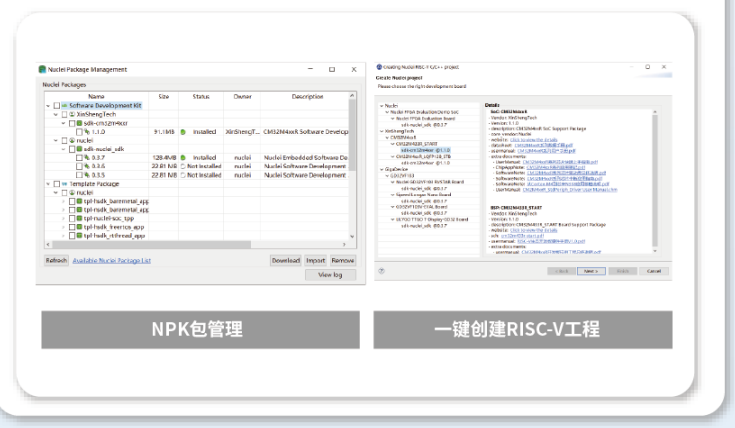
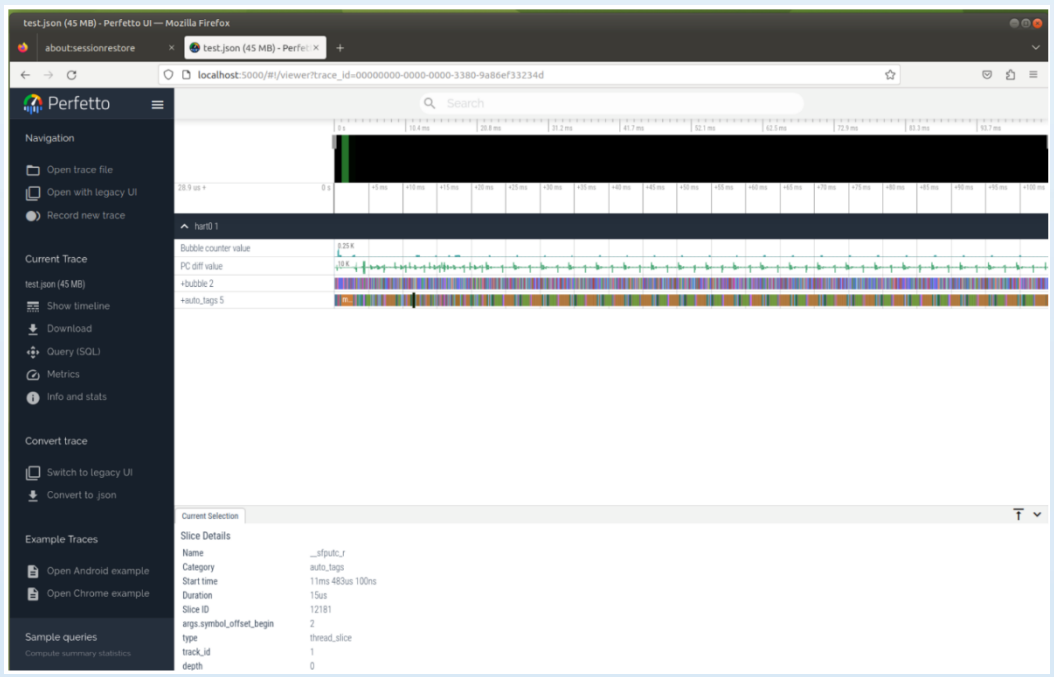
## Nuclei IDE

Eclipse CDT Based development environment, easy hands on with manual.

- Nuclei RISC-V GCC, OpenOCD and QEMU integrated
- Nuclei Package(NPK) software solution
- Support SoC Subsystem SDK one-click import
- Portable executables, without installation
- One-click project template
- One-click project configuration
- In system debugging and programming
- Integrated serial port tool
- Real time register display
- Support Linux and Windows
- Deeply integrated with RV Prof – professional performance profiling and optimizing tool，instruction and cycle level accurate
- Embedded with RISC-V e-trace，debug and analyze performance with ATB2AXI module and trace decoder




## NA300 Has Been Deployed to Automotive Applications

ADAS　Lidar　Engine ECU

MCU　Gateway　Computing