Nuclei RISC-V Processor

200 Series Product Brief

Nuclei N200 Series Product Brief

芯来科技 NUCLEI

Overall Introduction

Nuclei N200 Series is a 32b embedded processor based on RISC-V architecture that is compatible with **RV32I(E)MACB/Zc**. N200 Series features a **2-stage, in order pipeline**.

N200 Series consumes extreme low power with 1.80/4.7(legal/best) Dhrystone/MHz, 3.85 Coremark/MHz.

N200 Series supports both instruction and data local memory **(ILM/DLM)** gives better real time processing capability. User can also configure instruction cache **(I-Cache).**

N200 Series supports various RISC-V extensions, including **NICE(Nuclei Instruction Co-unit Extension), PMP and standard JTAG/cJTAG debug interface**.

N200 Series is designed for extreme low power applications like MCU and AIoT.

Extreme Low Power

RV32I(E)MACB/Zc

2-stage Pipeline Single Issue

Machine/User/ Supervisor Mode

PMP Security Features

AHB-Lite System Bus

RISC-V Standard Debug

4-Wire JTAG 2-Wire cJTAG

Low Latency Interrupt

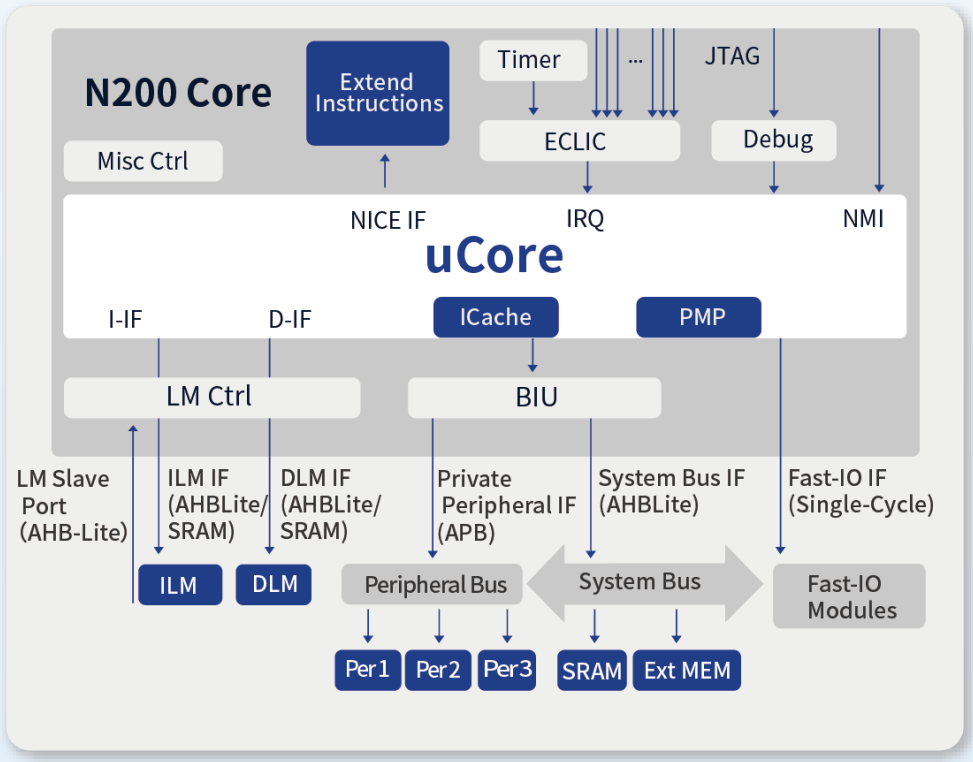
Full Dev Kit & SDK

Nuclei N200 Series Product Brief

芯来科技 NUCLEI

N200 Features

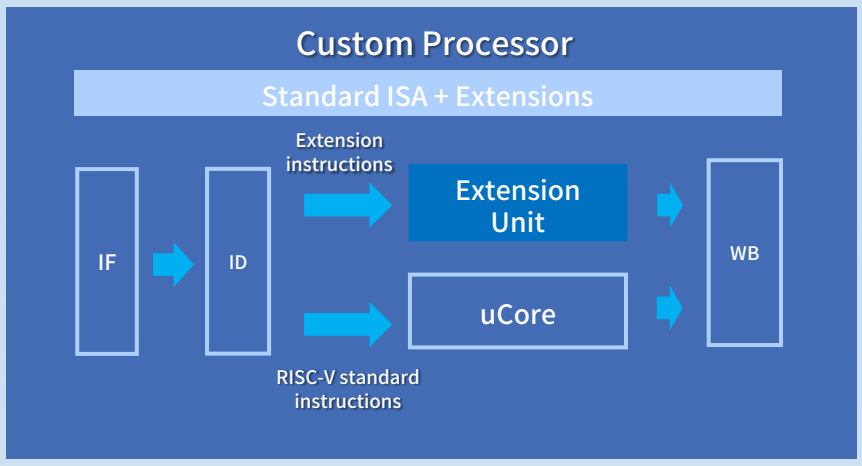
- RV32I(E)MACB/Zc compatible;
- Single Issue, in-order 2 stage pipeline;
- Support fast interrupts tail-chaining mechanism, vectored interrupt processing and software dynamically programmable division of interrupt levels and priorities; Provide advanced low latency interrupt feature for real-time application;
- Support Custom Instruction Extension(NICE);
- Configurable ILM (Instruction Local Memory) & DLM (Data Local Memory);
- Configurable I-Cache with Scratchpad mode;
- Support PMP for system security requirement;
- Support standard JTAG & cJTAG interface and Linux/Windows debug tools;
- Support standard RISC-V GNU toolchain and Linux/Windows dev environment (IDE)



N200 NICE Custom Instruction Extension

- All Nuclei processor IPs support NICE(Nuclei Instruction Co-unit Extension)，allowing customization capability;
- Combine customized hardware co-processor with N200, providing DSA better performance with low power;
- Embed customized instructions only use Intrinsic Function;

1. Define user-define instructions
2. Implement Extension Unit
3. Develop Domain Specific Lib/Function
4. Accelerate Domain Specific Applications



N200 Memory Subsystem

N200 Series supports local instruction and data memory: **ILM (Instruction Local Memory) 和DLM (Data Local Memory)**, providing real-time processing capability:

- ILM and DLM can be configured from **128B-2GB**, allowing excellent flexibility;
- **AHB-Lite interface and SRAM interface** with customized **address space.**

N200 Series supports Instruction Cache

- **2-way, 32B cache line** structure
- Cache size from **1KB-64KB**
- If ILM is not configured, I-Cache can be configured to **Scratchpad Mode** through CSR
- Support cache line **LOCK and INVAL** operation

N200 System Interface Introduction

Bus Interface	Description	Atomic Support	Burst Support	Cacheablility	Protocols	Bus Width
System Bus	System Instruction and Data	Yes	Yes	Configurable	AHB-Lite/AXI	32 bit
I-Cache Bus	Used for I-Cache miss	No	Yes	Configurable	AHB-Lite	32 bit
ILM Interface	Local Instruction	No	No	No	SRAM/ AHB-Lite	32 bit
DLM Interface	Local Data	No	No	No	SRAM/ AHB-Lite	32 bit
PPI Interface	Private Peripherals	No	No	No	AHB-Lite	32 bit
Slave Interface	External Master Read	No	No	No	AHB-Lite	32 bit

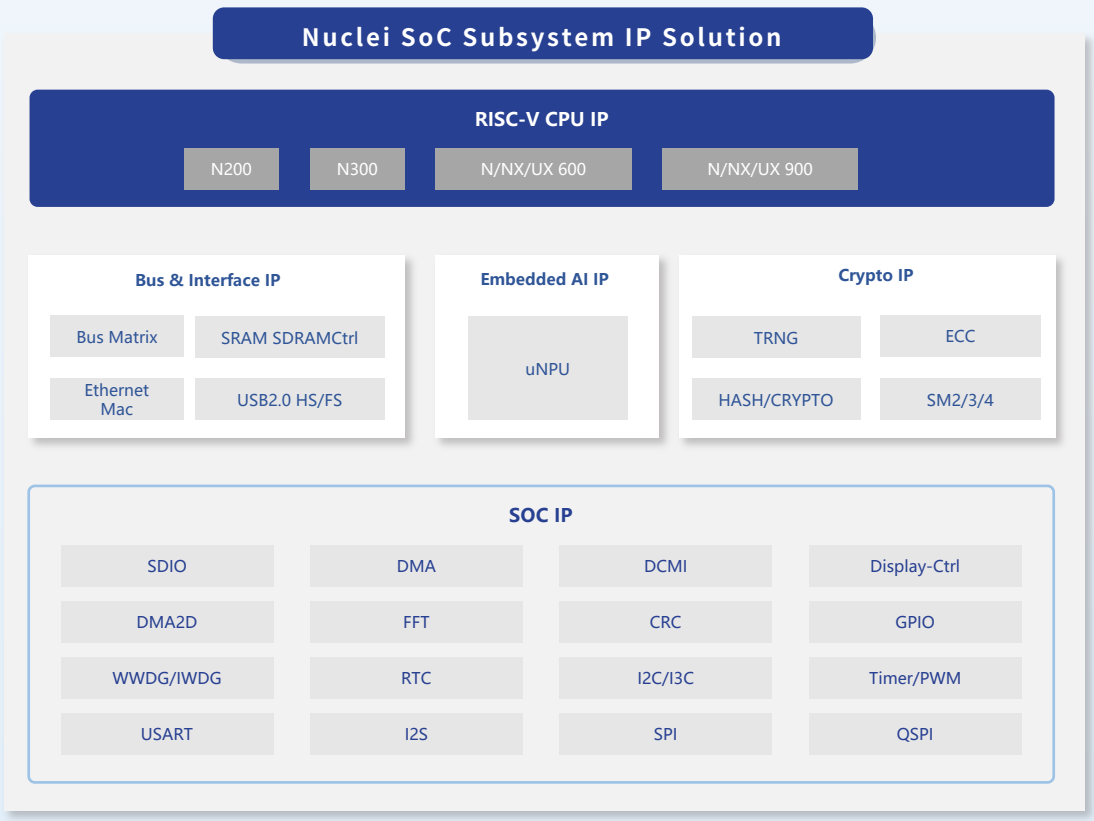
Nuclei N200 Series Product Brief

芯来科技 NUCLEI

Nuclei CPU Subsystem

Using internal tools from Nuclei to integrate CPU IPs with other peripheral IPs , verify and deliver **a full subsystem solution** to customer.

- Save money：Full subsystem IP **reduces customer's cost**;
- Save time：Fully customized SoC subsystem **saves customer's development cycle**;
- Save effort：Related SoC driver and SDK help **fast prototype bring up**.

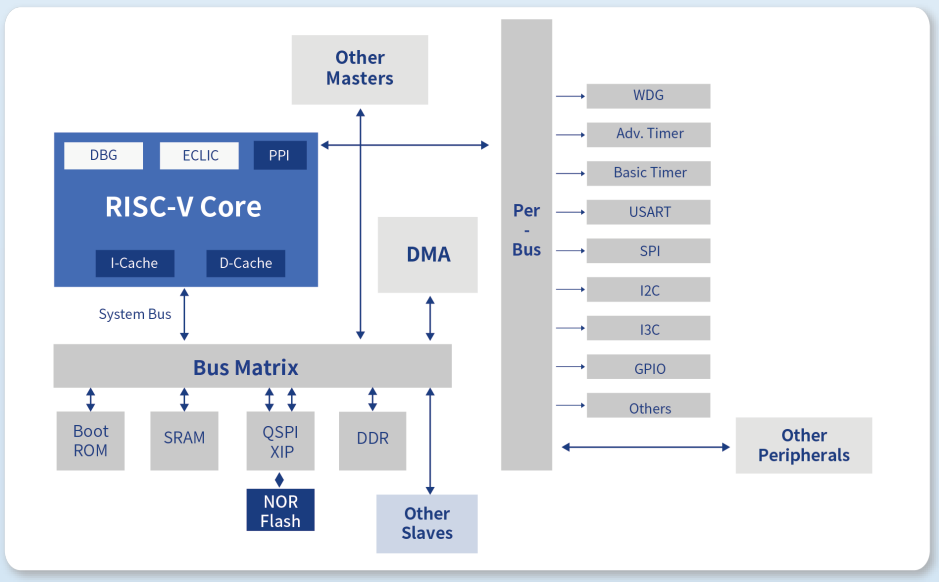


Innovative Subsystem IP Use Case

Use Case #1

Single-core：

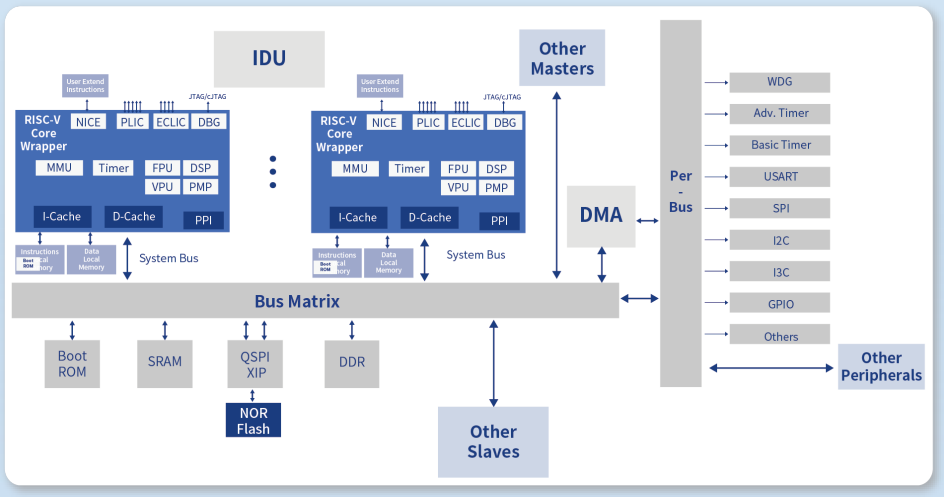
Customer succeeded to **bring up in 2 weeks** based on delivered IP package & SDK



Use Case #2

Multi-core：

Supported two modes **(real-time & application),** including IDU, bus matrix, etc.



Nuclei N200 Series Product Brief

芯来科技 NUCLEI

Nuclei IDE

Eclipse CDT Based development environment, easy hands on with manual.

- Nuclei RISC-V GCC, OpenOCD and QEMU integrated
- Nuclei Package(NPK) software solution
- Support SoC Subsystem SDK one-click import
- Portable executables, without installation
- One-click project template
- One-click project configuration
- In system debugging and programming
- Integrated serial port tool
- Real time register display
- Support Linux and Windows

N200 Series Has Been Deployed to Various Applications

AIoT

Communication

Storage

MCU

Connectivity

GNSS